

CLAIMS

What is claimed is:

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1. A method of generating test data to functionally verify a circuit, the method comprising:

detecting a data selection signal;

responsive to the data selection signal, presenting test data to verify the circuit,

wherein the presenting of the test data includes composing the test data utilizing a combination of algorithmically generated data and stored data.
2. The method of claim 1 wherein the composing of the test data is performed utilizing state machine generated data.
3. The method of claim 1 wherein the presenting of the test data is performed under the control of a state machine.
4. The method of claim 1 wherein the test data comprises a data stream.

5. The method of claim 4 wherein the data stream comprises a video test pattern to functionally test a video device.

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6. The method of claim 1 wherein the test data comprises a plurality of packets of data.

7. The method of claim 1 wherein the test data is supplied to a system to test functionality of the system.

8. The method of claim 7 wherein the system is a video display system.

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9. The method of claim 8 wherein the video display system comprises any one of a group of including a SMPTE-259M, SMPTE-292M and a Digital Video Interface (DVI) device.

10. The method of claim 1 further comprising utilizing the test data to perform built-in self-test of the circuit in parallel with the functional verification of the circuit.

11. The method of claim 10 further comprising feeding the test data to the circuit and to a checksum generator circuit.

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12. The method of claim 11 further comprising comparing an output of the checksum generator circuit to an expected checksum.
13. The method of claim 12 wherein the comparison is performed at a selected point within the test data.
14. The method of claim 1 wherein the circuit comprises part of a host system, and the test data is fed to the host system.
15. The method of claim 14 wherein the host system comprises a digital television system.
16. A test circuit to generate test data to functionally verify a subject circuit, the test circuit comprising:
 - a selection input to receive a data selection signal;
 - a test data generator, responsive to the data selection signal, to output test data to verify the circuit,wherein the test data generator is to compose the test data utilizing a combination of algorithmically generated data and stored data.

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17. The test circuit of claim 16 wherein the test data generator is to compose the test data utilizing state machine generated data.

18. The test circuit of claim 16 wherein presentation of the test data is performed under the control of a state machine of the test data generator.

19. The test circuit of claim 16 wherein the test data comprises a data stream.

20. The test circuit of claim 19 wherein the data stream comprises a video test pattern to functionally test a video device.

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21. The test circuit of claim 16 wherein the test data comprises a plurality of packets of data.

22. The test circuit of claim 1 further comprising a test data output to supply the test data to a system to test functionality of the system.

23. The test circuit of claim 22 wherein the system is a video display system.

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24. The test circuit of claim 23 wherein the video display system comprises any one of a group of including a SMPTE-259M, SMPTE-292M and a Digital Video Interface (DVI) device.
25. The test circuit of claim 16 further comprising built-in self-test circuitry to utilize the test data to perform a built-in self-test of the circuit in parallel with the functional verification of the subject circuit utilizing the output of the subject circuit generated responsive to the input of the test data.
26. The test circuit of claim 25 further comprising feeding the test data to the circuit and to a checksum generator circuit.
27. The test circuit of claim 26 further comprising comparing an output of the checksum generator circuit to an expected checksum.
28. The test circuit of claim 27 wherein the comparison is performed at a selected point within the test data, the selected point being determined by a state machine.
29. The test circuit of claim 16 wherein the subject circuit comprises part of a host system, and the test data is fed to the host system.

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30. The test circuit of claim 14 wherein the host system comprises a digital television system.

31. A method of testing a circuit comprising:

providing test data to the circuit, the test data functionally to verify the circuit, wherein the functional verification of the circuit is performed utilizing an output of the circuit generated responsive to the test data in accordance with operational functionality of the circuit; and

providing the test data to a built-in self-test (BIST) circuit in parallel with the provision thereof to the circuit, wherein the built-in self-test generates a BIST output responsive to the test data.

32. The method of claim 31 wherein the built-in self-test circuit includes a checksum generator, and the method includes comparing an output of the checksum generator to an expected checksum.

33. The method of claim 32 including retrieving the expected checksum from storage associated with the built-in self-test circuit.

34. The method of claim 33 comprising retrieving the expected checksum from a lookup table.

35. The method of claim 32 wherein the built-in self-test circuit includes a built-in self-test state machine.

36. The method of claim 35 wherein the built-in self-test state machine initiates the comparison of the output of the checksum generator to the expected checksum at a selected point in the test data.

37. The method of claim 31 wherein the functional verification is performed utilizing an output of a system including the circuit.

38. The method of claim 37 wherein the system comprises a digital video device, and where the output of the system is viewable on a video display to functionally verify the system.

39. The method of claim 38 wherein the output defines a test pattern.

40. A test system comprising:

a test data generator to provide test data to a subject circuit, the test data functionally to verify the subject circuit, wherein the functional verification of the subject circuit is performed utilizing an output of the subject circuit generated responsive to the test data in accordance with operational functionality of the subject circuit; and

a built-in self-test (BIST) circuit to receive the test data concurrently with the provision thereof to the subject circuit.

41. The test system of claim 40 wherein the built-in self-test circuit includes a checksum generator and compares an output of the checksum generator to an expected checksum.

42. The test system of claim 41 wherein the built-in self-test circuit is to retrieve the expected checksum from storage associated with the built-in self-test circuit.

43. The test system of claim 42 wherein the built-in self-test circuit is to retrieve the expected checksum from a lookup table.

44. The test system of claim 40 wherein the built-in self-test circuit includes a built-in self-test state machine.

45. The test system of claim 41 wherein the built-in self-test state machine is to initiate a comparison of the output of the checksum generator to the expected checksum at a selected point in the test data.

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~~45.~~ The test system of claim 40 wherein the functional verification is performed utilizing an output of a system including the subject circuit.

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~~46.~~ The test system of claim 45 wherein the system comprises a digital video device, and where the output of the system is viewable on a video display to functionally verify the system.

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~~47.~~ The test system of claim 46 wherein the output defines a test pattern.

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~~48.~~ A method of manufacturing a test circuit to generate test data to functionally verify a subject circuit, the method comprising:

constructing a selection input to receive from a data selection

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signal,

coupling a test data composer to an algorithmic data generator
and to a data storage unit,

coupling the selection input to a test data generator so as to
enable the test data composer, responsive to the data selection signal,
to output test data to verify the circuit, the test data generator to
compose the test data utilizing a combination of algorithmically
generated data retrieved from the algorithmic data generator and
stored data retrieved from the data storage unit.

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A method of manufacturing a test system, the method
comprising:

providing a test data generator to provide test data to a subject
circuit, the test data functionally to verify the subject circuit,
wherein the functional verification of the subject circuit is
performed utilizing an output of the subject circuit generated
responsive to the test data in accordance with an operational
functionality of the subject circuit; and

coupling the test data generator to a built-in self-test (BIST)

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circuit so as to enable the built-in self-test circuit to receive the test data concurrently with the provision thereof to the subject circuit.

1. The circuit of claim 1, wherein the built-in self-test circuit is configured to receive the test data concurrently with the provision thereof to the subject circuit.